Embedded 32-bit Microprocessor Core KVARC

Microprocessor core KVARC is a 32-bit RISC general purpose embedded MPU. It is a proprietary design of Russian company KM211, part of KM Core international group of companies. The core is a high efficiency, low power, low gatecount processor, ARM 9/ARM 11 class.

Application

- Handheld devices:
  - Palm devices
  - System-on-Chip (SoC) for navigation systems
  - Reader IC for e-passports, ID, bank smart-cards and goods tags
- DSP and multimedia devices:
  - Digital TV, set-top-box
  - SoC for digital high bandwidth surveillance cameras
- Data transfer protection:
  - Crypto-IC for radio units
  - Network router with national cryptography support
  - USB ID for PC users
- Industrial/Signal control
- Automotive:
  - SoC for car security
  - Vehicle black-box, video-registrator (needed for insurance cases)
- Military, avionics
- Medical

Why KVARC?

- Native russian advanced design (energy efficiency of best level)
- Documentation is fully in accordance with russian national standards and requirements
- Original instruction set makes it hard to copy the design
- Open approach, no undocumented functioning and backdoors
- RTL is provided by licensing agreements
- SOI production is possible, high quality requirements testing is possible
- Flexible licensing, reasonable licensing quotes
- No foreign companies licensing spendings
- National economy investment, further core evolvement

Classical architecture

- RISC, Harvard
- 32-bit operands
- 4GByte address space
- 5-stage pipeline
- Most instructions are single cycle
- Static branch prediction
- MMU with automatic page loading
- 32-bit system bus

Performance-energy efficiency of class of ARM 9/ARM 11

- Over 400 MHz at 90nm.
- 1.1 DMIPS/MHz
- High energy efficiency of 8.5 DMIPS/mW (compared to ARM946E-E 1.19 DMIPS/MHz & 8.6 DMIPS/mW)
- Multiply-accumulate (MAC) 16x16, 2 cycles
- DSP — extension of instruction set
- High density 32/16 bit instruction set mixture
- FPU SP/DP — optional block of floating point arithmetics, single/double precision
- Optional multimedia codec:
  - Video MPEG2 coding-decoding
  - Video MPEG4 coding-decoding
  - Audio MP3 coding-decoding
- Low-power sleep modes

Very small gatecount and as a result cost-efficiency of IC's based on KVARC core

Target	Device	Area	Performance
ASIC	TSMC 90 nm	0,2 mm^2 (70K gates) — w/o cache & MMU	> 400 MHz
		2 mm^2 (450K gates) — with 48Kb cache (32+16) & MMU	
FPGA	Xilinx Virtex 4	2000 slices — w/o cache & MMU	60 MHz
	Altera Cyclone IV	7150 LEs — w/o cache & MMU	60 MHz

Suitable for signal control

- Low interrupt latency of 6 cycles
- No-caches and MMU version of the core is available to run just firmware without operating system (a much smaller gatecount and power consumption)
- High configurability
- Additional commands support in ISA or on peripheral blocks level

Ease and speed of software development and competitive SoC development workflow

- Ported Linux 2.6
- C-compiler (GNUGCC)
- FPGA target support, can debug a final system on FPGA
- SDK for Windows/Linux, based upon open source Eclipse
- Software models for new projects can be developed by any external developers due to open source-based SDK tools

A set of available peripheral and interface modules

- Networking: Ethernet
- LCD-controller
- Smart-cards and ID interfaces: ISO7816, ISO14443
- GPIO, timers, PWMs,CRC-calculation
- Flash controllers: NAND, compact-flash
- Serial interfaces: USART, I^2C, I^2S, SPI

Other IP-blocks are applicable via AMBA interface bus (under development)

Data protection and chip integrity

- RSA (1024,2048 bit)
- EC-DSA (160-1024 bit)
- DSA
- AES
- DES/3DES
- Final design can support a number of sensors for protection:
  - Metal grid
  - Voltage sencor
  - Internal generator, floating clock
  - Photo-sensor

High level of maturity — passed tapeout.

Deliverables

#	Document	Soft IP	Firm IP
1	Core IP datasheet (functional description, structure, Interface description, programming guide)	+	+
2	Electrical and timing specs	–	–
3	Verilog RTL description	+	–
4	Verilog Netlist	–	+
5	Synthesis scripts	+	–
6	Timing constraints file(.sdc)	–	+
7	GNUGCC compiler and source codes for it	+	+
8	GNU toolchain: GNUGDB debugger, linker, source codes	+	+
9	Ported C library GlibC, source codes	+	+
10	Ported Linux 2.6, source codes	+	+

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